UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/788,596	02/21/2001	Hirokazu Miyazaki	PA-1136	8771

466 7590 09/24/2003

YOUNG & THOMPSON
745 SOUTH 23RD STREET 2ND FLOOR
ARLINGTON, VA 22202

EXAMINER
PAREKH, NITIN

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 09/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No.	Applicant(s)	
	09/788,596	MIYAZAKI, HIROKAZU	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Peri d for R ply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,12-14 and 18-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,7,9,12,13,18-21 and 25* is/are rejected.

7)☒ Claim(s) *5, 8, 14 and 22-24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 February 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claim 24 is objected to because of the following informalities:

Claim 24, line 2: Delete "elongate".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.**

3. Claims 12 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Kitahara (US Pat. 5440452).

Regarding claim 12, Kitahara discloses an insulating tape/sheet (4/41 in Fig. 16, 17 and 1-3d) provided between a semiconductor chip and a wiring substrate (1 and 7 respectively in Fig. 16) comprising:

- a plurality of holes/windows (44 Fig. 1) there through
- a plurality of leads (3 in Fig. 1 and 16) on a first surface of the tape, the leads having two ends including a fixed end (left portion 3/31 of the lead on
- right side of the chip in Fig. 16) and an other end (right portion 32/33 of the lead on right side of the chip in Fig. 16)

- the other end having a variety of shapes comprising a hanging shape or shaped to be afloat in the hole (32/33 in Fig. 2-3d; Col. 7, line 15, 65 and Col. 8, line 25) and being protruded from the second surface of the insulating sheet (32 in Fig. 2-3c; Col. 5, line 50), and
- the plurality of connection bumps (11 in Fig. 2) being electrically connected through the fixed end and the other end of the lead to corresponding connection pads on the wiring substrate/board (Fig. 17; Col. 6, line 37)

(Fig. 16, 17 and 1-3d; Col. 5, line 20- Col. 6, line 60; Col. 7 and 8).

Regarding claim 13, Kitahara teaches substantially the entire claimed structure as applied to claim 12 above, wherein Kitahara teaches the other end of the lead being protruded from the second surface through the hole (32 in Fig. 2-3c; Col. 5, line 50).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-4, 6, 7, 9, 18-21 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khandros et al. (US Pat. 5448266) in view of Miyazaki et al (US Pat. 6342726).

Regarding claim 1, Khandros et al. disclose a mounting structure of a semiconductor package comprising:

- a semiconductor chip (28 in Fig. 2) which is provided with a plurality of electrical contacts/bump pads (40 in Fig. 2)
- a wiring substrate (20 in Fig. 2) which is provided with a plurality of contact/ connection pads (24 in Fig. 2)
- an interposer/insulating sheet (42 in Fig. 2) having apertures/holes (54 in Fig. 2; Col. 7, lines 33-40)) there through at positions corresponding to the contact/connection pads and terminals of a plurality of leads (48/50 in Fig. 2; Col.), the interposer/insulating sheet being made of material such as polyimide resin/polymer (Col. 14, line 25)
- interposer/insulating sheet being provided between the chip and the wiring substrate, and
- the plurality of electrical contacts/bump pads being electrically connected through the leads and solder mass/bumps to corresponding contact/connection pads on the wiring substrate (Col. 7, lines 25-33)

(Fig. 1-8, Col. 6, line 55- Col. 12, line 25).

Khandros et al. further teach:

- the plurality of electrical contacts/bump pads on the chip being arranged in the entire area of the chip including a peripheral and central regions (Col. 8, line 25)
- the electrical contacts/bump pads being disposed at equal spacing/pitch (Col. 8, line 27) throughout the entire area forming a pattern/array corresponding to a grid pattern of terminals (48 in Fig. 2) and contact/connection pads on the wiring substrate (see a portion of the grid pattern in Fig. 5A/5B; Col. 16, line 46), and
- the grid pattern/array of the terminals and contact/connection pads on the wiring substrate being out of vertical alignment with that electrical contacts/bump pads on the chip (see Fig. 2).

Khandros et al. fail to teach the electrical contacts/bump pads of the chip being solder balls.

Miyazaki et al. teach using a semiconductor chip having pads/bumps in a variety of conventional contact structures such as solder balls, stud bumps, etc. (43/45 in Fig. 44 and 47 respectively; Col. 21, line 50- Col. 22, line 45).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the chip provided with a plurality of solder balls as

taught by Miyazaki et al. so that the interconnect integrity, strength and reliability can be improved in Khandros et al's structure.

Regarding claim 2, Khandros et al. and Miyazaki et al. teach substantially the entire claimed structure as applied to claim 1 above, wherein Khandros et al. teach the interposer/insulating sheet having apertures/holes (54 in Fig. 2) there through at positions corresponding to the connection pads and terminals.

Regarding claims 3 and 4, Khandros et al. and Miyazaki et al. teach substantially the entire claimed structure as applied to claim 1 above, wherein Khandros et al. further teach one end of each of the leads being fixed (48 in Fig. 5B) on a first surface of the interposer/ insulating sheet (46 in Fig. 5B) while the other end of each of the leads being shaped to be afloat in the respective hole (see 56 in the hole 54 in Fig. 5B) and further being protruded from the second surface of the interposer/insulating sheet (see Fig. 2 and 3).

Regarding claim 6, Khandros et al. and Miyazaki et al. teach substantially the entire claimed structure as applied to claims 1 and 4 above, wherein Khandros et al. teach each of the plurality of electrical contacts/bump pads being electrically connected through the other end of the leads and solder mass/bumps to corresponding contact/connection pads on the wiring substrate (Col. 7, lines 25-33).

Regarding claim 7, Khandros et al. and Miyazaki et al. teach substantially the entire claimed structure as applied to claims 1 and 4 above, wherein Khandros et al. further teach the leads being formed of conductive/resilient material such as copper, gold, etc. (Col. 14, lines 45-50).

Regarding claim 9, Khandros et al. and Miyazaki et al. teach substantially the entire claimed structure as applied to claims 1 and 4 above, wherein Khandros et al. teach the interposer/insulating sheet being made of material such as polyimide resin/polymer (Col. 14, line 25).

Regarding claim 18, Khandros et al. disclose a mounting structure of a semiconductor package comprising:

- a semiconductor chip (28 in Fig. 2) which is provided with a plurality of electrical contacts/bump pads (40 in Fig. 2) on a chip surface
- a wiring substrate (20 in Fig. 2) which is provided with a plurality of contact/ connection pads (24 in Fig. 2)
- an interposer/insulating sheet (42 in Fig. 2) having apertures/holes (54 in Fig. 2; Col. 7, lines 33-40)) there through at positions corresponding to the
- contact/connection pads and terminals of a plurality of leads (48/50 in Fig. 2; Col.), the interposer/insulating sheet being made of material such as polyimide resin/polymer (Col. 14, line 25)

- interposer/insulating sheet being located intermediate/between the chip and the wiring substrate, and
- the plurality of electrical contacts/bump pads being electrically connected through the leads and solder mass/bumps to corresponding contact/connection pads on the wiring substrate (Col. 7, lines 25-33) (Fig. 1-8, Col. 6, line 55- Col. 12, line 25).

Khandros et al. further teach:

- the plurality of electrical contacts/bump pads on the chip being arranged in the entire area of the chip including a peripheral and central regions (Col. 8, line 25)
- the electrical contacts/bump pads being disposed at equal spacing/pitch (Col. 8, line 27) throughout the entire area forming a first pattern/array corresponding to a grid pattern of terminals (48 in Fig. 2) and contact/connection pads on the wiring substrate (see a portion of the grid pattern in Fig. 5A/5B; Col. 16, line 46), and
- the grid pattern/array of the terminals and contact/connection pads on the wiring substrate being out of vertical alignment with that electrical contacts/bump pads on the chip (see Fig. 2).

Khandros et al. fail to teach the array/pattern comprising the electrical contacts/bump pads of the chip being solder balls.

Miyazaki et al. teach using a semiconductor chip having pads/bumps in a variety of conventional contact structures such as solder balls, stud bumps, etc. (43/45 in Fig. 44 and 47 respectively; Col. 21, line 50- Col. 22, line 45).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the chip provided with a plurality of solder balls as taught by Miyazaki et al. so that the interconnect integrity, strength and reliability can be improved in Khandros et al's structure.

Regarding claim 19, Khandros et al. and Miyazaki et al. teach substantially the entire claimed structure as applied to claim 18 above, wherein Khandros et al. further teach the grid array/pattern comprising three rows of array positions (see three rows of 40/48/24 in Fig. 2).

Regarding claim 20, Khandros et al. and Miyazaki et al. teach substantially the entire claimed structure as applied to claim 18 above, wherein Khandros et al. teach the interposer/insulating sheet having apertures/holes (54 in Fig. 2), the leads passing through the apertures/holes and the fixed end/portion of the leads (48 in Fig. 2) being in electrical contact with the electrical contacts/bump pads and also being in contact with a surface of the interposer/insulating sheet.

Regarding claim 21, Khandros et al. and Miyazaki et al. teach substantially the entire claimed structure as applied to claims 18 and 19 above, except the hole corresponding to each row in the insulating sheet being an elongate.

Miyazaki et al. teach using a tape substrate having a variety of configurations of openings/holes including the opening/hole having an elongate shape (see 23 in Fig. 9) to accommodate a plurality of leads (Col. 18, lines 1-40).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the hole corresponding to each row in the insulating sheet having an elongate shape as taught by Miyazaki et al. so that the lead density can be increased and processing can be simplified in Khandros et al's structure.

Regarding claim 25, Khandros et al. and Miyazaki et al. teach substantially the entire claimed structure as applied to claim 18 above, wherein Khandros et al. further teach at least some of the contact/connection pads being located within a boundary/vertical extension of a perimeter of the chip (see 24 under the perimeter of the chip 28 in Fig. 1).

Allowable Subject Matter

6. Claims 5, 8, 14, 22-24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter.

The primary reason for an allowance of claims 5, 8, 14, 22-24 is the inclusion of the limitations a mounting structure of a semiconductor package comprising a semiconductor chip provided with a first pattern of a grid array of solder balls, a wiring substrate having a corresponding first pattern of a grid array of connection pads where the pattern of the connection pads being out of vertical alignment with that of the solder balls, an insulating sheet having holes there through and leads passing through the holes and connecting the solder balls and the connection pads. The mounting structure is further configured such that a fixed end of the lead is in contact with the solder balls and also with a surface of the insulating sheet and the holes are filled with a resin such that a space between the solder balls is free of the resin.

The prior art references Khandros et al. (US Pat. 5448266), Miyazaki et al (US Pat. 6342726) and DiStefano et al. (US Pat. 5518964) lack teachings of having the mounting structure where the insulating sheet having holes there through and leads passing through the holes is configured such that the fixed end of the lead is in contact with the solder balls and also with a surface of the insulating sheet while the other end is connected to the wiring substrate through the holes, the holes further are sealed with a resin in a manner that the space between the solder balls is free of the resin.

Response to Arguments

8. Applicant's arguments with respect to claims 1-4 and 6, 7 and 9 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 703-305-3410. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3431.

Nitin Parekh

NP
09-14-03

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800